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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,198	01/28/2004	Shinichi Saito	HITA.0501	1130

7590 08/24/2005

REED SMITH LLP
Suite 1400
3110 Fairview Park Drive
Falls Church, VA 22042

EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,198	SAITO ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/28/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3-4 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Madurawe (US. 2004/0152245).

Regarding claim 1, Madurawe (Fig. 4) discloses a semiconductor device, comprising: a silicon on insulator (SOI) substrate having an insulating layer 407 and a monocrystalline silicon layer 480 (par. [0058], lines 1-4) formed on a base substrate 400; a source diffusion portion 413 and a drain diffusion portion 414 both formed of a first conductive type and formed from the monocrystalline silicon layer 480 on the surface layer of the SOI substrate; a channel portion 406 also formed from the monocrystalline layer 480 and also of the first conductive type (par. [0040]) having one end adjacent to the source diffusion portion 413 of the first conductive type and the

other end adjacent to the drain diffusion portion 414 of the first conductive type; and a gate insulating film 405 formed on the channel portion 406.

Regarding claims 3-4 and 6, Madurawe's Fig. 4 further discloses that the channel portion 406 is fully depleted (par. [0049], lines 1-6) and has an impurity concentration lower than the concentration of a source/drain impurity (par. [0040]), and no junction between the first conductive type and a second conductive type opposite to the first conductive type is formed in the monocrystalline silicon layer 480.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 7-10, 11-13 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madurawe (US. 2004/0152245) in view of Ma et al (US. 6,060,755).

Regarding claims 2, 8-10 and 17-19, Madurawe (Fig. 4) discloses a semiconductor device, comprising: a silicon on insulator (SOI) substrate having an insulating layer 407 and a monocrystalline silicon layer 480 (par. [0058], lines 1-4) formed on a base substrate 400; a source diffusion portion 413 and a drain diffusion portion 414 both formed of a first conductive type and formed from the monocrystalline silicon layer 480 on the surface layer of the SOI substrate; a channel portion 406 also formed from the monocrystalline layer 480 and also of the first conductive type (par. [0040]) having one end adjacent to the source diffusion portion 413 of the first

conductive type and the other end adjacent to the drain diffusion portion 414 of the first conductive type; and a gate insulating film 405 formed on the channel portion 406.

Madurawe does not disclose the gate insulating film 405 is a laminated film comprising an insulating film and a metal oxide film having a higher dielectric constant than the insulating film.

However, Ma (Figs. 12-13) teaches a semiconductor device including a laminated gate insulating film comprising: an insulating film 62 of silicon oxynitride (column 6, lines 1-6), and a metal oxide film 56 consisting of hafnium or zirconium and having a higher dielectric constant than the insulating film 62 (column 5, lines 51-59). Accordingly, it would have been obvious to modify the device structure of Madurawe by forming the gate insulating film 405 with a laminated insulating film as set forth above because such laminated insulating film would increase the electron mobility and reduced the electrical leakage of the MOSFET, as taught by Ma (column 1, lines 49-54).

Regarding claims 7 and 16, Madurawe further discloses that the thickness Ts of the monocrystalline silicon layer 480 (see Fig. 4) can be optimized to contain the fully depleted channel (par. [0058]), the thickness Ts of the silicon layer 480 needs to be less than the depletion depth Xd (Ts<Xd) (see EQ 4 and par. [0059]).

Regarding claim 11, as discussed in details above, Fig. 4 of Madurawe substantially reads on the invention as claimed. Madurawe (Fig. 14) further discloses the forming of a CMOS on the SOI substrate, the CMOS comprising NMOS disposed in a first area and PMOS disposed in a second area (par. [0154]), the first area is

separated from the second area by a separating area made from an insulating material formed in the SOI substrate (see Fig. 14).

Regarding claims 12-13 and 15, Madurawe's Fig. 4 further discloses that the channel portion 406 is fully depleted (par. [0049], lines 1-6) and has an impurity concentration lower than the concentration of a source/drain impurity (par. [0040]), and no junction between the first conductive type and a second conductive type opposite to the first conductive type is formed in the monocrystalline silicon layer 480.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Madurawe (US. 2004/0152245) in view of Imai et al (US. 5,847,419).

Madurawe does not disclose the channel 406 comprising a stack of first and second monocrystalline semiconductor layers as claimed.

However, Imai (Fig. 3K) teaches the forming of NMOSFET on the SOI substrate, the NMOSFET having a channel SOI layer 15/16 comprising a first semiconductor layer 15 of SiGe and a second semiconductor layer 16 of Si formed on the first semiconductor layer 15, wherein a first lattice constant of the first semiconductor 15 and a second lattice constant of the second semiconductor differ from each other to form a strained silicon portion in the channel portion (column 8, lines 42-45). Accordingly, it would have been obvious to modify the device structure of Madurawe by forming the channel 406 with a laminated semiconductor layer as set forth above because such laminated channel semiconductor layer would provide an increasing of a mobility in the electron channel, as taught by Imai (column 5, lines 60-67 through column 6, lines 1-2).

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Madurawe and Ma et al as applied to claim 2 above, and further in view of Imai et al (US. 5,847,419).

Neither Madurawe nor Ma discloses the channel comprising a stack of first and second monocrystalline semiconductor layers as claimed.

However, Imai (Fig. 3K) teaches the forming of NMOSFET on the SOI substrate, the NMOSFET having a channel SOI layer 15/16 comprising a first semiconductor layer 15 of SiGe and a second semiconductor layer 16 of Si formed on the first semiconductor layer 15, wherein a first lattice constant of the first semiconductor 15 and a second lattice constant of the second semiconductor differ from each other to form a strained silicon portion in the channel portion (column 8, lines 42-45). Accordingly, it would have been obvious to modify the device structure of Madurawe by forming the channel 406 with a laminated semiconductor layer as set forth above because such laminated channel semiconductor layer would provide an increasing of a mobility in the electron channel, as taught by Imai (column 5, lines 60-67 through column 6, lines 1-2).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
August 19, 2005

PHAT X. CAO
PRIMARY EXAMINER